

in contact with the low tunnel barrier intergate insulator and a metal layer formed on the control gate and also in contact with the low tunnel barrier intergate insulator, wherein the metal layers are selected from the group consisting of platinum (Pt) and aluminum (Al).

38. (Original) The method of claim 35, wherein erasing charge from the one or more floating gates by tunneling electrons off of the floating gate and onto the number of control gates further includes:

providing a negative voltage to a substrate of one or more DEAPROM memory cells; and
providing a large positive voltage to the control gate for the one or more DEAPROM memory cells.

39. (Original) The method of claim 38, wherein the method further includes erasing an entire row of DEAPROM memory cells by providing a negative voltage to all of the substrates along an entire row of DEAPROM memory cells and providing a large positive voltage to all of the control gates along the entire row of DEAPROM memory cells.

40. (Original) The method of claim 38, wherein the method further includes erasing an entire block of DEAPROM memory cells by providing a negative voltage to all of the substrates along multiple rows of DEAPROM memory cells and providing a large positive voltage to all of the control gates along the multiple rows of DEAPROM memory cells.

41. (New) The vertical memory cell of claim 10, wherein the control gate has a tunnel barrier of less than 1.5 eV.

42. (New) The vertical memory cell of claim 10, wherein the control gate is adapted for a Dynamic Electrically Alterable Programmable Read Only Memory.